REMARKS

By this amendment, claims 1-2, 5-6, 8, 11-12, and 15-16 have been amended. Claim 4 has been withdrawn from the application. Claims 1-17 are pending in the application. Applicants reserve the right to pursue the original claims and other claims in this and other applications.

Claims 5, 8, 11-12, and 15-16 have been amended to correct typographical errors and/or to clarify the invention.

Claims 1-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tomita et al. (US 5,457,661). This rejection is respectfully traversed.

Claim 1, as amended, recites a method of reading data from a memory array comprising, *inter alia*, "transferring a plurality of data bits from a memory array onto respective input/output signal lines; and sensing at least one of said data bits on a first input/output signal line at a first timing and sensing another of said data bits on a second input/output signal line at a second timing different from said first timing, wherein said sensing timing is related to a capacitance associated with said first and second input/output signal lines" (emphasis added). Tomita et al. does not disclose these limitations. As noted in the Office Action, Tomita et al. discloses in the background section that if "the wiring resistance and wiring capacity are increased to an unignorable extent, ... the result [is] that the timing at which data is latched is delayed more and more." Col. 2, ln. 50-52. This is described as a drawback of conventional memory devices. Col. 2, ln. 53. Tomita et al. discloses an undesirable delay as a side-effect of the wiring. Therefore, Tomita et al. teaches away from sensing timing related to a capacitance associated with said first and second input/output signal lines, as recited in claim 1. Tomita et al. does not disclose how data is sensed at all.

Since Tomita et al. does not disclose all the limitations of claim 1, claim 1 is not anticipated by Tomita et al.

Claim 6, as amended, recites a column output delay circuit for a memory device comprising, *inter alia*, "a first delay device, said first delay device delaying a column enable signal for a first period of time based on a capacitance of a first input/output signal line; and a second delay device, said second delay device delaying a column enable signal for a second period of time based on a capacitance of a second input/output signal line" (emphasis added). Tomita et al. does not disclose these limitations. Tomita et al. discloses that "NOR gate 25 receives both an output signal of the NAND gate 23 and a signal generated by delaying the output signal of the gate 23 by the two inverters 24." Col. 5, ln. 1-4 (emphasis added). There is no first or second delay device delaying a column enable signal for a period of time based on a capacitance of a respective first or second input/output signal line, as recited in claim 6. Since Tomita et al. does not disclose all the limitations of claim 6, claim 6 is not anticipated by Tomita et al.

Claims 9 and 14 recite a memory device comprising, *inter alia*, "a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of at least two input/output signal lines, when the at least two input/output signal lines are sensed by said sense amplifiers" (emphasis added). Tomita et al. does not disclose this limitation. Tomita et al. discloses that "NOR gate 25 receives both an output signal of the NAND gate 23 and a signal generated by delaying the output signal of the gate 23 by the two inverters 24." Col. 5, ln. 1-4 (emphasis added). There is no column output delay circuit for controlling, based on a capacitance of at least two input/output signal lines, when the input/output signal lines are sensed by the sense amplifiers, as recited in claims 9 and 14. Since Tomita et al. does not

disclose all the limitations of claims 9 and 14, claims 9 and 14 are not anticipated by Tomita et al.

Claims 2-5 depend from claim 1 and are patentable at least for the reasons mentioned above. Claims 7-8 depend from claim 6 and are patentable at least for the reasons mentioned above. Claims 10-13 depend from claim 9 and are patentable at least for the reasons mentioned above. Claims 15-17 depend from claim 14 and are patentable at least for the reasons mentioned above. Applicants respectfully request that the 35 U.S.C. § 102(b) rejection of claims 1-17 be withdrawn.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Dated: December 22, 2005

Respectfully submitted,

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